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3D Simulation of coaxial carbon nanotube field effect transistor

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Abstract. We provide a model of coaxial CNTFET geometry. Coaxial devices are of special interest because their geometry allows for better electrostatics. We explore the possibilities of using non-equilibrium Green's function method to get I-V characteristics for CNTFETs. This simulator also includes a graphic user interface (GUI) of Matlab. We review the capabilities of the simulator, and give examples of typical CNTFET's 3D simulations (current-voltage characteristics are a function of parameters such as the length of CNTFET, gate thickness and temperature). The obtained I-V characteristics of the CNTFET are also presented by analytical equations.

Keywords: CNT, carbon nanotube, CNTFET, NEGF, I-V characteristics.

1. Introduction

The carbon nanotube field-effect transistor (CNTFET) is a promising candidate for future electron devices. Rapid progress in the field has recently made it possible to fabricate CNTFET based circuits, such as logic gates, static memory cells, and ring oscillators.

This three-terminal device consists of a semiconducting nanotube bridging two contacts (source and drain) and acting as a carrier channel, which is turned on or off electrostatically via the third contact (gate). Presently, there are various groups pursuing the fabrication of such devices in several variations, achieving increasing success in pushing performance limits, while encountering myriad problems, as expected for any technology in its infancy.

Manufacturing issues will ultimately play a decisive role in any future CNT electronic technology. It is still too early to tell what role CNTFETs will play in electronic systems of the future, but they provide us with a specific context in which to develop technology and understand transport, contacts, interfaces, etc., which are likely to be important for CNT electronics in general. It is appropriate, however, to say a few words about where CNTFET technology stands today. Early CNTFETs were fabricated using nanotubes synthesized by a laser ablation process using nickel-cobalt catalysts. The nanotubes were then suspended in a solvent and dispersed on an oxidized silicon wafer with predefined metal contact pads. The result was a random distribution of CNTs some of which bridged the contacts. Subsequently, catalytic chemical vapor deposition (CVD) methods were developed to grow CNTs on predefined catalyst islands [1]. The nanotubes thus fabricated are rooted in the catalyst islands and grow in random directions on the wafer. Some CNTs terminate on another island and create the bridges. CVD techniques provide more control over device fabrication and have led to rapid progress in device performance.

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CNTFETs are typically p-type devices that operate as so-called Schottky barrier (SB) transistors. The p-type characteristics have been attributed to the alignment of source-drain metal Fermi level near the valance band of the CNTs rather than to background doping or charges. The holes in the channel are electrostatically induced by applying a negative gate voltage. Transistor action occurs because the gate modulates the SB width for hole tunnelling near metal-CNT contact. While early transistors used gold (Au) as contact metals, significant performance improvements were obtained by using palladium contacts instead, which seem to eliminate the Schottky barrier for holes and produce near-ballistic operation [2].

Early CNTFETs were fabricated on oxidized silicon substrates with a back-gated geometry and a thick SiO_2 layer that resulted in poor gate control of drain current.

The use of a top-gated geometry produced immediate performance improvements [3]. Wind *et al.* deposited a thin dielectric layer (15-20 nm) on top of CNTs, and lithographically defined metal electrodes for gating and contacts. A transconductance ($g_m = dI_{ds}/dV_{gs}|_{Vds}$) of 3.25 μS and subthreshold swing ($S = ln\ (10)\ [dV_{gs}/d\ (ln\ (I_{ds}))]$) of 130 mV/decade were obtained, which was a significant improvement in device performance. Later, the incorporation of high-κ dielectrics in a top-gated structure produced even better device characteristics. Javey *et al.* employed a high-κ ZrO_2 (κ ~ 25) gate dielectric with a thickness of ~ 8 nm and obtained $g_m \approx 12$ μS and $S \approx 70$ mV/decade [4]. Although not always with top-gated geometry, other groups have also reported the use of high-κ dielectrics such as HfO_2 (κ ~ 11), TiO_2 (κ ~ 40-90), $SrTiO_3$ (κ ~ 175), and even electrolyte gating mechanisms for attaining improved performances. In the case of electrolyte gating, Siddon *et al.* have reported $S \approx 62$ mV/decade which is very close to the theoretical limit of 60 mV/decade. All of these devices appear to operate as CNT MSDFETs, some with essentially no barrier and others with rather large (half band gap) barriers.

Several recent improvements to CNTFET design collectively incorporate various techniques that have been developed during the past few years. For instance, Javey *et al.* reported a self-aligned top gate structure that uses the catalytic CVD method for CNT growth, a thin. HfO_2 top gate dielectric ~50 nm in length and self-aligned palladium source/drain contacts. A transconductance of 30 μS, subthreshold swing of 110 mV/decade, and a saturation current of ~25 μA at a power supply of V_{DS}~1 V were obtained. Novel CNTFET device structures that enable high current operation and high integration densities have also been reported. These devices are all of the metal source-drain (MSDFET) variety, but it is recognized that the use of a metal source will limit the drain current (unless the SB is sufficiently negative). Very recently, CNT MOSFETs with doped source/drain regions have been reported [5, 6]. Substitutional doping is not practical because of the strong carbon-carbon bond, so charge transfer approaches analogous to modulation doping in III-V heterostructures are used.

Although progress in CNTFETs has been rapid, there are still many issues to discuss. The potential for digital logic was demonstrated early on. Techniques that modify the behaviour of the nanotube from p-type to n-type have been implemented, which allowed their use in complementary CMOS logic. Following this, Derycke *et al.* demonstrated an inverter structure based on nanotubes. Other nanotube based elementary digital logic gates with high gain and high I_{on}/I_{off} ratios, such as a NOR gate, a ring oscillator and an SRAM cell, have also been implemented [7, 8].

In this work, we start with a brief summary of progress in CNTFET technology since the first reports in 1998. This discussion is intended to provide background for whom not familiar with CNTFET technology. As our understanding of CNTFET device physics has evolved, an ability to model and simulate them has also been developed. We also briefly describe the device simulation approach that we use. We provide a model of coaxial CNTFET geometry. Coaxial devices are of special interest because their geometry allows for better electrostatics than their planar counterparts. Capitalizing on the inherent cylindrical shape of nanotubes, these devices would exhibit wrap-around gates that maximize capacitive coupling between the gate electrode and the nanotube channel.

In this work, we also review the capabilities of the simulator, summarize the theoretical approach and experimental results, and give examples of typical CNTFET's 3D simulations (current-voltage characteristics are a function of parameters such as the length of CNTFET, the gate thickness and temperature). The obtained I-V characteristics of the CNTFET are also presented by analytical equations.

2. Simulation results

2.1 Coaxial CNTFET geometry

We now provide a brief description of typical CNTFET geometries, which are grouped in two major categories, planar and coaxial. A CNTFET, whether planar or coaxial, relies on similar principles, while being governed by additional phenomena such as 1D density of states (DOS) and ballistic transport. The coaxial geometry maximizes the capacitive coupling between the gate electrode and the nanotube surface, thereby inducing more channel charge at a given bias than other geometries. This improved coupling is desirable in mitigating the short-channel effects that plague technologies like CMOS as they downsize device features. It is also of importance to low-voltage applications a dominating trend in the semiconductor industry and to allow, potentially, for easier integration with modern implementations of existing technologies such as CMOS. Besides the wrap around gate, special attention must also be paid to the geometry of the end contacts, since these play a role in determining the dimensions of the Schottky barriers that are present in the channel near the device ends and have a direct effect on current modulation. We hereinafter deal specifically with the coaxial geometry of the CNTFET shown in figure 1, but we note that most concepts and results discussed in this work are still transferable to planar devices, at least in a qualitative sense. The key device dimensions are: the gate inner radius, R_g, and thickness, t_g; the nanotube radius, R_t, and length L_t; the insulator thickness $t_{ins} = R_g - R_t$; the end-contact radius, t_c (the source and drain may sometimes be of different sizes), and length, L_c; and the gate-underlap L_u. Note that a closed-cylinder structure was employed for simplicity in treating the electrostatics, wherein $L_c = t_g = L_u = 0$, $t_c = R_g$ and $L_g = L_t$.

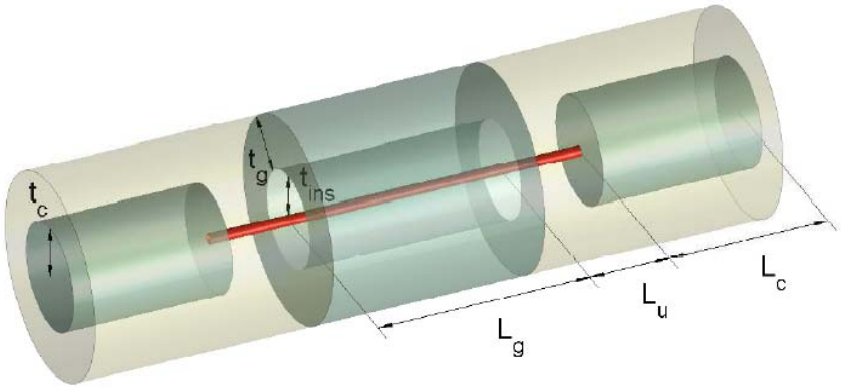

Figure 1. Coaxial CNTFET structure. The insulator fills the entire simulation space not occupied by metal or the nanotube [9].

2.2 Review of the NEGF formalism

A carbon nanotube can be viewed as a rolled-up sheet of graphene with a diameter typically between one and two nanometers. The nanotube can be either metallic or semiconducting, depending on how it is rolled up from the graphene sheet (i.e. depending on its chirality). Semiconducting nanotubes are suitable for transistors. In order to correctly treat carbon nanotube transistors, strong quantum confinement around the tube circumferential direction, quantum tunnelling through Schottky barriers

at the metal nanotube contacts, and quantum tunnelling and reflection at barriers in nanotube channel need to be considered. The non-equilibrium Green's function (NEGF) formalism, which solves Schrödinger equation under non-equilibrium conditions and can treat coupling to contacts and dissipative scattering process, provides a sound basis for quantum device simulations. The NEGF simulation approach has demonstrated its usefulness for simulating nanoscale transistors from conventional Si MOSFETs, MOSFETs with novel channel materials, to CNTFETs [10], and molecular transistors [11]. In this section, we give brief summary of the NEGF simulation procedure. For a more thorough description of the technique one can refer to reference [12]. Figure 2 shows a generic transistor and defines some terms for the NEGF simulation.

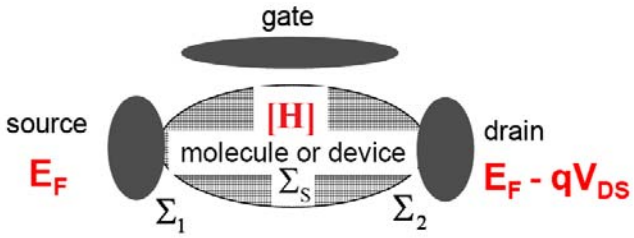

Figure 2. The generic transistor with a molecule or device channel connected to the source and drain contacts. The source-drain current is modulated by a third electrode, the gate. The quantities in the NEGF calculation are also shown.

The first step is to identify a suitable basis set and Hamiltonian matrix for an isolated channel. The self-consistent potential, which is a part of the Hamiltonian matrix, is included in this step. The second step is to compute the self-energy matrices, Σ_1, Σ_2 and Σ_S, which describe how the ballistic channel couples to the source/drain contacts and to the scattering process. For simplicity, only ballistic transport is treated in this work. After identifying the Hamiltonian matrix and the self-energies, the third step is to compute the retarded Green's function,

$$\mathbf{G}(E) = [(E + i0+)\,\mathrm{I} - \mathbf{H} - \Sigma_1 - \Sigma_2]^{-1} \tag{1}$$

The fourth step is to determine the physical quantities of interest from the Green's function. In the ballistic limit, states within the device can be divided into two parts: 1) states filled by carriers from the source according to the source Fermi level, and 2) states filled by the drain according to the drain Fermi level. Within the device, the source (drain) local-density-of-states (LDOS) is $\mathbf{D}_{S(D)} = \mathbf{G}\Gamma_{S(D)}\mathbf{G}^{+}$, where $\Gamma_{S(D)} = I(\Sigma_{1(2)} - \Sigma_{1(2)}^{+})$ is the energy level broadening due to the source (drain) contact. The charge density within the device is computed by integrating the LDOS, weighted by the appropriate Fermi level over energy. The charge contributed by the source contact is

$$Q_S(z) = (-e)\int_{E_N}^{+\infty} D_S(E,z) f(E - E_{FS})dE + e\int_{-\infty}^{E_N} D_S(E,z)\{1 - f(E - E_{FS})\}dE \ , \tag{2}$$

where e is the electronic charge and E_N is the charge neutrality level. The total charge is:

$$Q(z) = Q_S(z) + Q_D(z) = (-e)\int_{-\infty}^{+\infty} dE \cdot \mathrm{sgn}[E - E_N(z)]\{D_S(E,z) f(\mathrm{sgn}[E - E_N(z)](E - E_{FS}))$$

$$+ D_D(E,z) f(\mathrm{sgn}[E - E_N(z)](E - E_{FD}))\}, \tag{3}$$

where sgn (E) is the sign function, and $E_{FS,D}$ is the source (drain) Fermi level. For a self-consistent solution, the NEGF transport equation is solved with iteratively the Poisson equation until self-consistency is achieved after which the source-drain current is computed from formula

$$I = \frac{4e}{h}\int T(E)[f_S(E) - f_D(E)]dE \quad , \tag{4}$$

where T (E) = Trace ($G_1G^+_2$) is the source-drain transmission and the extra factor of two comes from the valley degeneracy in the carbon nanotube energy band structure. The computationally expensive part of the NEGF simulation is finding the retarded Green's function, according to equation (1), which requires the inversion of a matrix for each energy grid point. The straightforward way is to explicitly invert the matrix, whose size is the size of the basic set. This, however, is impractical for an atomistic simulation of a nanotube transistor. In the ballistic limit, the problem is simplified because only a few columns of the Green's function are needed. Still, reducing the size of the Hamiltonian matrix and developing computationally efficient approaches are of great importance for an atomistic simulation.

2.3 Main screen of coaxial CNTFET

Purpose of the project was to make a user-friendly simulator that provides as much control as possible over every aspect of the simulation. Consequently, graphic user interface (GUI) development in Matlab was a major part of the programme. Here we present an overview of the most important GUI features.

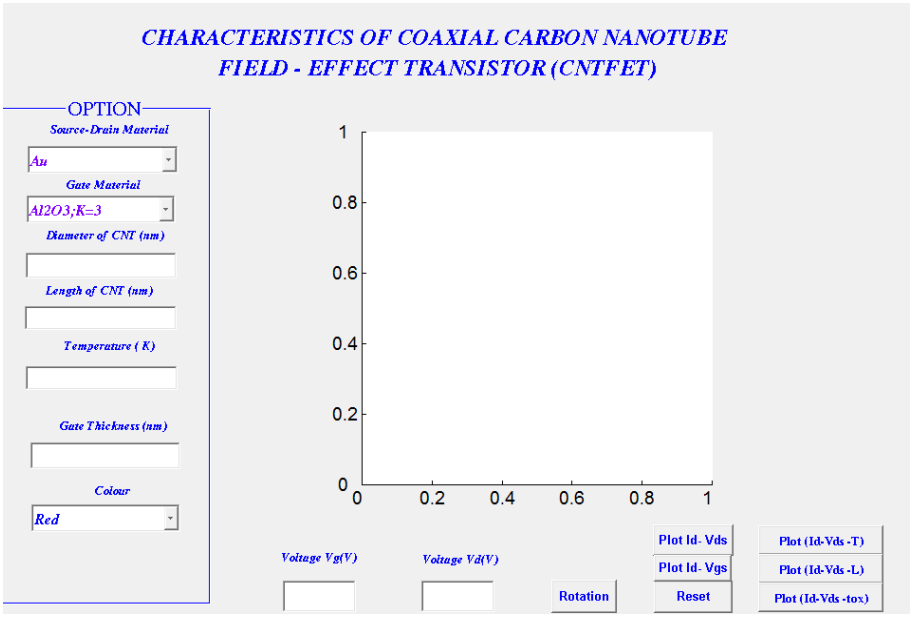

Figure 3. The main screen of simulation programme of coaxial CNTFET. Source-drain material (Au), Gate material (Al_2O_3, k = 3), Colour (Red) are default settings.

The main screen shown in figure 3 is the central location where one can control the simulation program. From main screen, one can quickly enter simulation parameters with minimum of typing. Clicking the left mouse pointer on each item of the main screen to enter the parameters such as types of source-drain materials (Au, Pt, Pd); types of gate materials (Al_2O_3 (k = 5), HfO_2 (k = 20), ZrO_2 (k = 26), TiO_2 (k = 65), $SiTiO_3$ (k = 175)); length of CNT (nm); temperature (K); gate thickness (nm); colours (blue, green, pink, yellow, black); voltage V_g (V); V_d (V). Clicking the right mouse pointer on the item which is used to calculate the current voltage characteristics in 2D (plot I_d-V_{ds} or plot I_d-V_{gs}), reset used to clear current data or in 3D (plot I_d-V_{ds}-T, Plot I_d-V_{ds}-L and plot I_d-V_{ds}-t_{ox}). During calculation, symbol "running" will be appeared. Source-drain material (Au), Gate material (Al_2O_3, k = 3), Colour (Red) are default settings. Simulations in 2D take less time than in 3D. Thanks to simulations in 3D, one can get more information of tendency and effects of parameters such as temperature, the length of CNT, the gate thickness on I-V characteristics.

2.4 Simulations of current-voltage characteristics of coaxial CNTFET

The drain I-V characteristics in 2D are shown in figure 4. The saturation current at V_{GS} = 0.5 V is around 6 μA, which is not inconsistent with values emerging from recent experimental work [13].

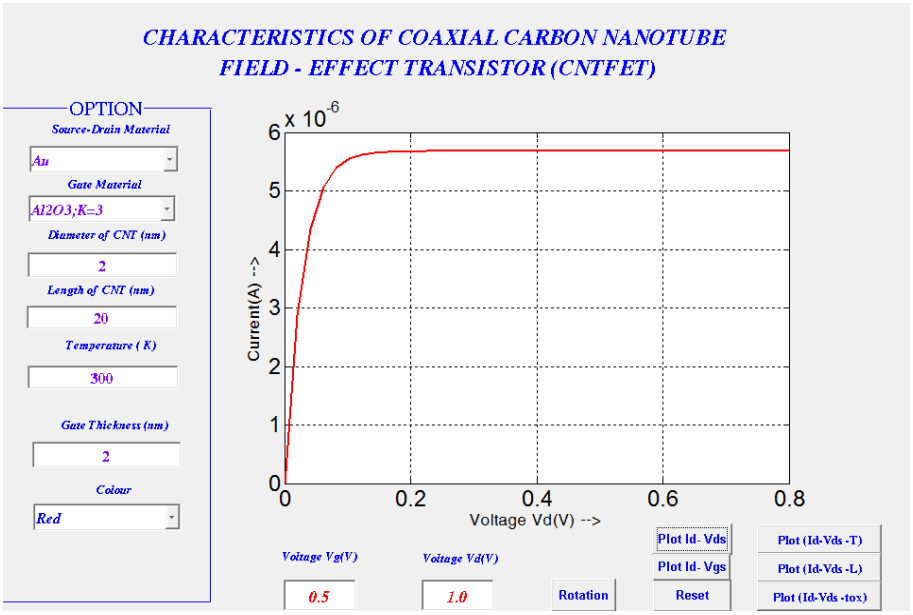

Figure 4. Drain current-voltage characteristics of coaxial CNTFET.

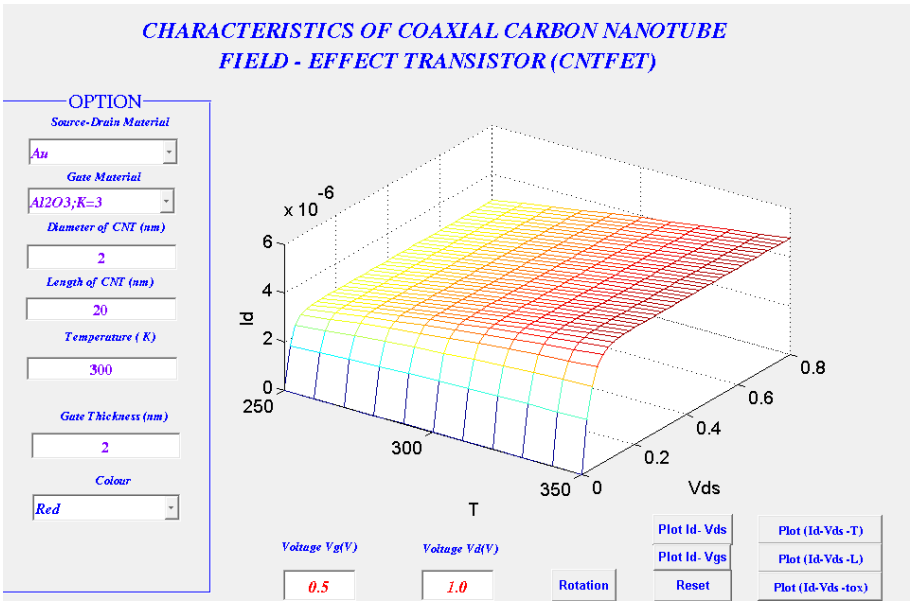

Figure 5. Drain current-voltage characteristics in 3D. When CNTFET is cooled, its saturation drain currents were lightly decreased.

The drain I-V characteristics in 3D are shown in figure 5. The parameters used in 3D simulation were drain current-voltage characteristics and temperature. Drain I-V characteristics exhibited dependence of saturation drain current on temperature. When CNTFET is cooled, saturation currents were lightly decreased.

Drain current-voltage characteristics in 3D exhibited dependence of saturation currents on CNTFET length L are shown in figure 6. Tendency of saturation currents is decreased, when CNTFET

length is increased.

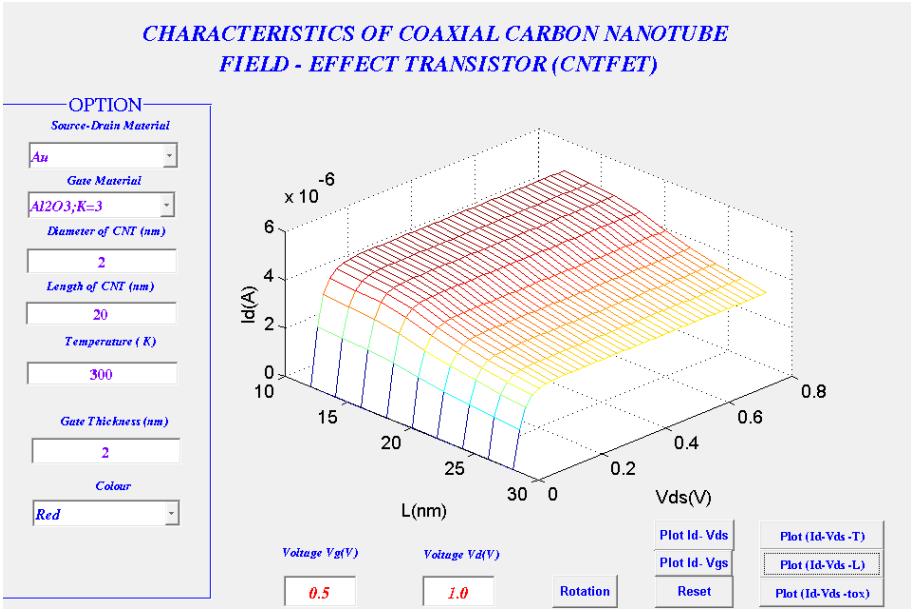

Figure 6. Drain current-voltage characteristics in 3D exhibited dependence of saturation drain currents on CNTFET length.

Drain current-voltage characteristics in 3D exhibited dependence of saturation current on the gate thickness of CNTFET, t_{ox} are shown in figure 7.

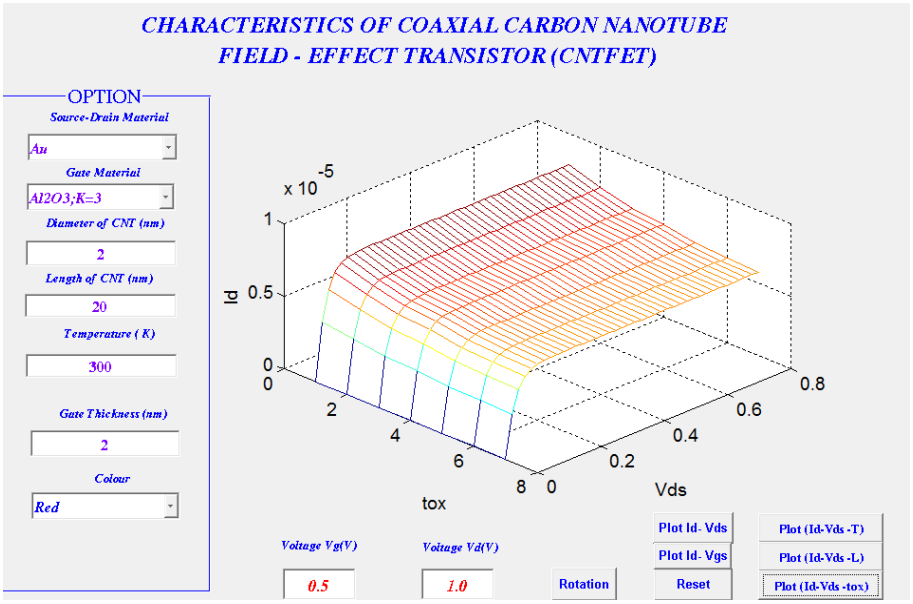

Figure 7. Drain current-voltage characteristics in 3D exhibited dependence of saturation drain currents on the gate thickness of CNTFET.

The current voltage curve can be divided into two regions: linear and saturation. Drain current in the linear region of CNTFET can be described as follows:

$$I_d = \mu C_{ox}[(V_{gs} - V_T)V_{ds} - \frac{V_{ds}^2}{2}], \quad (5)$$

or

$$I_d = K_n\left[2\left(V_{gs} - V_T\right)V_{ds} - V_{ds}^2\right], \tag{6}$$

where K_n is conductance of CNTFET, μ is mobility of carriers, C_{ox} is gate capacitance.

In the coaxial CNTFET

$$C_{ox} = 2\pi R_g L_g k\varepsilon_0\left(\lg\frac{R_g}{R_t}\right)^{-1}, \tag{7}$$

where k is relative dielectric constant, ε_0 is dielectric constant in vacuum, $8.85\times10^{-14}\mathrm{Fcm}^{-2}$.

We can also obtain saturation current of CNTFET by replacing $V_{ds(sat)} = V_{gs} - V_T$. Then the expression of saturation current of CNTFET can be written as follows:

$$I_{d(sat)} = K_n\left(V_{gs} - V_T\right)^2 . \tag{8}$$

3. Conclusions

A coaxial model for CNTFET has been proposed, which is specially intended for 3D simulations of drain current-voltage characteristics. The proposed model has been verified and a good agreement with recent experimental data [13] is found. A set of 3D simulations was then successfully performed for different parameters of materials, the length, the gate thickness of CNTFET, and temperature. The effects of these parameters on I-V characteristics have been predicted. Analytical equations of drain current-voltage curve are also presented.

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